WHAT IS CLAIMED IS:

1. A printhead, comprising:
   a) a data receiver and a data driver, said data receiver and data driver being coupled to a common data pad;
   b) a clock pad;
   c) a data bus;
   d) a shift register comprising a plurality of storage elements chained between said data receiver and said data driver, wherein:
      i) at least one of said storage elements is coupled to said clock pad;
      ii) outputs of a first number of said storage elements are coupled to said data bus; and
      iii) a second number of said storage elements comprise first and second data inputs, of which said first data inputs form a part of said shift register, and said second data inputs are coupled to said data bus; and
   e) a select line coupled to said second number of storage elements for switchably coupling either of said first or said second data inputs of said second number of storage elements to outputs of said second number of storage elements.

2. A printhead as in claim 1, further comprising
   a) a start line;
   b) a disable line; and
   c) a start bit comparator, said start bit comparator comprising:
      i) at least one input coupled to an output of at least one of said plurality of storage

elements;

ii) an output coupled to said start line; and

iii) a disable input for carrying a signal which is determined in part by the state of said start line.

3. A printhead as in claim 2, further comprising a clear line coupled to those of said plurality of storage elements having outputs coupled to said start bit comparator.

4. A printhead as in claim 3, further comprising:

a) a latch line; and

b) a plurality of latches coupled to said latch line;

wherein said outputs of said first number of storage elements are coupled to inputs of said latches, and outputs of said latches are coupled to said data bus.

5. A printhead as in claim 4, further comprising:

a) an enable line; and

b) a plurality of buffers coupled to said enable line;

wherein said outputs of said latches are coupled to inputs of said buffers, and outputs of said buffers are coupled to said data bus.

6. A printhead as in claim 4, further comprising a data driver enable circuit coupled between an output of said shift register and said data driver.

7. A printhead as in claim 6, further comprising:

a) a read/write comparator circuit;

b) a pen ID comparator circuit; and

c) control circuitry for:

i) placing said printhead in a listening mode by enabling said start bit comparator via said disable line;

ii) disabling said start bit comparator via said disable line, for a period of time after said start line is asserted;

iii) causing at least one read/write bit, at least one pen ID bit, and at least one address bit received by said first number of storage elements to be output to said data bus by asserting said latch line;

iv) if said at least one pen ID bit matches a pen ID of said printhead, and said at least one read/write bit is indicative of a write operation, causing at least one data bit received by said first number of storage elements to be output to said data bus and written to a location determined by said at least one address bit;

v) if said at least one pen ID bit matches a pen ID of said printhead, and said at least one read/write bit is indicative of a read operation, causing a number of data bits addressed by said at least one address bit to be placed on said data bus, and causing said select line to be asserted; and

vi) before a read or write operation is completed, causing said at least one read/write bit, said at least one pen ID bit, and said at least one address bit to be output from said printhead via said

data driver.

8. A printhead as in claim 7, wherein if said at least one pen ID bit matches a pen ID of said printhead, and said at least one read/write bit is indicative of a write operation, said control circuitry causes said at least one data bit which was written to a location determined by said at least one address bit to be read from said location and placed on said data bus, and thereafter causes said select line to be asserted.

9. A printhead as in claim 6, further comprising:

a) a pen ID comparator circuit; and

c) control circuitry for:

i) placing said printhead in a listening mode by enabling said start bit comparator via said disable line;

ii) disabling said start bit comparator via said disable line, for a period of time after said start line is asserted;

iii) causing at least one pen ID bit received by said first number of storage elements to be output to said data bus by asserting said latch line;

iv) if said at least one pen ID bit matches a pen ID of said printhead, and said printhead is conducting a write operation, causing at least one data bit received by said first number of storage elements to be output to said data bus and written to a register within said printhead;

v) if said at least one pen ID bit matches a pen ID of said printhead, and said

printhead is conducting a read operation, causing a number of data bits to be placed on said data bus, and causing said select line to be asserted; and

vi) before a read or write operation is completed, causing said at least one pen ID bit to be output from said printhead via said data driver.

10. A printhead as in claim 1, further comprising a data driver enable circuit coupled between an output of said shift register and said data driver.

11. A printhead as in claim 1, further comprising:

a) a latch line; and

b) a plurality of latches coupled to said latch line;

wherein said outputs of said first number of storage elements are coupled to inputs of said latches, and outputs of said latches are coupled to said data bus.

12. A printhead as in claim 11, further comprising:

a) an enable line; and

b) a plurality of buffers coupled to said enable line;

wherein said outputs of said latches are coupled to inputs of said buffers, and outputs of said buffers are coupled to said data bus.

13. A printhead, comprising:

a) a data receiver and a data driver, said data receiver and data driver being coupled to a common data pad;

b) a clock pad;

c) a data bus;

d) means for shifting data between said data receiver and said data driver in accordance with strobe signals received over said clock pad;

e) means for transferring data from said means for shifting to said data bus; and

f) means for transferring data from said data bus to said means for shifting.

14. A printhead as in claim 13, wherein:

a) said means for shifting data is a means for shifting serial data; and

b) said means for transferring data from said data bus to said means for shifting is a parallel data transfer means.

15. A printhead as in claim 13, wherein:

a) said means for shifting data is a means for shifting serial data; and

b) said means for transferring data from said means for shifting to said data bus is a parallel data transfer means.

16. Apparatus for printing, comprising:

a) a printer control unit;

b) a number of printheads;

c) a clock wire interconnecting the printer control unit and the number of printheads; and

d) a data wire interconnecting the printer control unit and the number of printheads;

e) wherein each of the number of printheads comprises:

i) a data receiver and a data driver, said data receiver and data driver being coupled to said data wire;

ii) a clock pad coupled to said clock wire;

iii) a data bus;

iv) a shift register comprising a plurality of storage elements chained between said data receiver and said data driver, wherein:

A) each of said storage elements is coupled to said clock pad;

B) outputs of a first number of said storage elements are coupled to said data bus; and

C) a second number of said storage elements comprise first and second data inputs, of which said first data inputs form a part of said shift register, and said second data inputs are coupled to said data bus; and

v) a select line coupled to said second number of storage elements for switchably coupling either of said first or said second data inputs of said second number of storage elements to outputs of said second number of storage elements.

17. A method of transmitting data between a printer control unit and a number of printheads, wherein said printer control unit and number of printheads are interconnected via a clock wire and a data wire, comprising the steps of:

a) transmitting a strobe signal over said clock wire;

b) said printer control unit transmitting at least

one start bit, at least one read/write bit, at least one pen ID bit, at least one address bit, and at least one data bit over said data wire; and

c) each of said number of printheads,

i) determining whether said at least one pen ID bit matches a pen ID of the printhead;

ii) if said at least one pen ID bit matches the pen ID of the printhead, retransmitting said at least one read/write bit, said at least one pen ID bit, and said at least one address bit over said data wire;

iii) if said at least one pen ID bit matches the pen ID of the printhead, and said at least one read/write bit is indicative of a write operation, causing said at least one data bit to be written to a location which is determined by said at least one address bit; and

iv) if said at least one pen ID bit matches the pen ID of the printhead, and said at least one read/write bit is indicative of a read operation, causing a number of data bits addressed by said at least one address bit to be transmitted over said data wire.

18. A method of accepting data transmitted by a printer control unit by a printhead assigned a pen ID and coupled to the printer control unit via a clock wire and a data wire, comprising the steps of:

accepting a strobe signed over the clock

wire

accepting at least one start bit, at least one read/write bit, at least one pen ID bit, at least one address bit, and at least one data bit over the data wire;

determining whether said at least one pen ID bit matches a pen ID of the printhead;

when said accepted at least one pen ID bit matches the pen ID of the printhead, retransmitting said accepted at least one read/write bit, said accepted at least one pen ID bit, and said accepted at least one address bit over said data wire; and

when said accepted at least one pen ID bit matches the pen ID of the printhead, and said accepted at least one read/write bit is indicative of a write operation, causing said accepted at least one data bit to be written to a printhead location which is determined by said accepted at least one address bit.

19. A method of accepting data transmitted by a printer control unit by a printhead assigned a pen ID and coupled to the printer control unit via a clock wire and a data wire, comprising the steps of:

accepting a strobe signal over the clock wire;

accepting at least one start bit, at least one read/write bit, at least one pen ID bit, at least one address bit, and at least one data bit over the data wire;

determining whether said at least one pen ID bit matches a pen ID of the printhead;

when said accepted at least one pen ID bit

matches the pen ID of the printhead, retransmitting said accepted at least one read/write bit, said accepted at least one pen ID bit, and said accepted at least one address bit over said data wire; and

when said accepted at least one pen ID bit matches the pen ID of the printhead, and said accepted at least one read/write bit is indicative of a read operation, causing a number of data bits addressed by said at least one address bit to be transmitted over said data wire.